THE DATASHEET OF

NTA4153NT1G

NTA4153N, NTE4153N, NVA4153N, NVE4153N

MOSFET – Single, N-Channel with ESD Protection, Small Signal, SC-75 and SC-89

20 V, 915 mA

ON Semiconductor®

http://onsemi.com

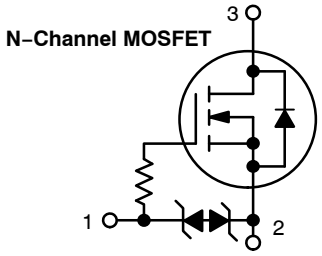
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
20 V	0.127 Ω @ 4.5 V	915 mA
	0.170 Ω @ 2.5 V	
	0.242 Ω @ 1.8 V	
	0.500 Ω @ 1.5 V	

Features

- Low $R_{DS(on)}$ Improving System Efficiency
- Low Threshold Voltage, 1.5 V Rated
- ESD Protected Gate
- NV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- Pb−Free Packages are Available

Applications

- Load/Power Switches
- Power Supply Converter Circuits
- Battery Management
- Portables like Cell Phones, PDAs, Digital Cameras, Pagers, etc.



MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Units
Drain−to−Source Voltage			V_{DSS}	20	V
Gate−to−Source Voltage			V_{GS}	±6.0	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	915	mA
		T_A = 85°C		660	
Power Dissipation (Note 1)	Steady State		P_D	300	mW
Pulsed Drain Current	t_p =10 μs		I_{DM}	1.3	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Continuous Source Current (Body Diode)			I_S	280	mA
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

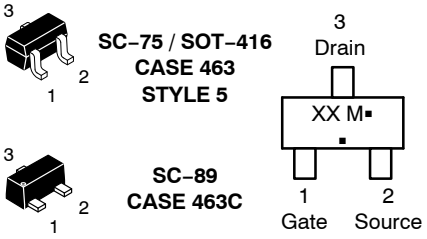
THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Units
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$		°C/W
SC−75 / SOT−416		416	
SC−89		400	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

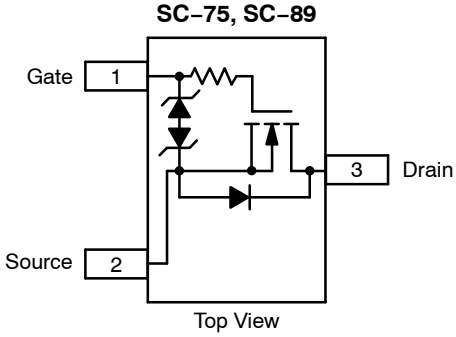
1. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

MARKING DIAGRAM & PIN ASSIGNMENT



XX = Device Code
M = Date Code*
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.



ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		20	26		V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				18.4		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 16 V				100	nA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±4.5 V				±1.0	μA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		0.45	0.76	1.1	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−2.15		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 600 mA			127	230	mΩ
		V_{GS} = 2.5 V, I_D = 500 mA			170	275	
		V_{GS} = 1.8 V, I_D = 350 mA			242	700	
		V_{GS} = 1.5 V, I_D = 40 mA			500	950	
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 400 mA			1.4		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 16 V			110		pF
Output Capacitance	C_{OSS}				16		
Reverse Transfer Capacitance	C_{RSS}				12		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 0.2 A			1.82		nC
Threshold Gate Charge	$Q_{G(TH)}$				0.2		
Gate−to−Source Charge	Q_{GS}				0.3		
Gate−to−Drain Charge	Q_{GD}				0.42		
SWITCHING CHARACTERISTICS (Note 3)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DD} = 10 V, I_D = 0.2 A, R_G = 10 Ω			3.7		ns
Rise Time	t_r				4.4		
Turn−Off Delay Time	$t_{d(OFF)}$				25		
Fall Time	t_f				7.6		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 200 mA	T_J = 25°C		0.67	1.1	V
			T_J = 125°C		0.54		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

TYPICAL ELECTRICAL CHARACTERISTICS

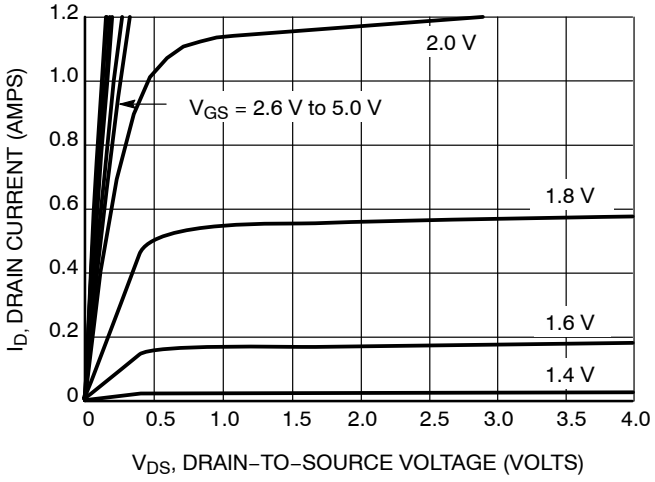


Figure 1. On−Region Characteristics

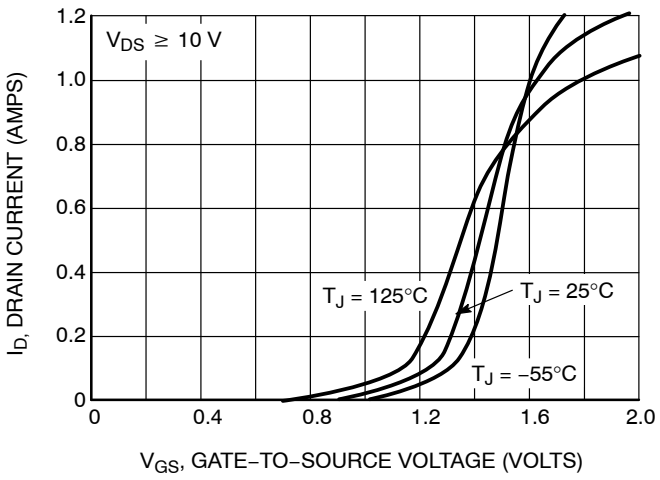


Figure 2. Transfer Characteristics

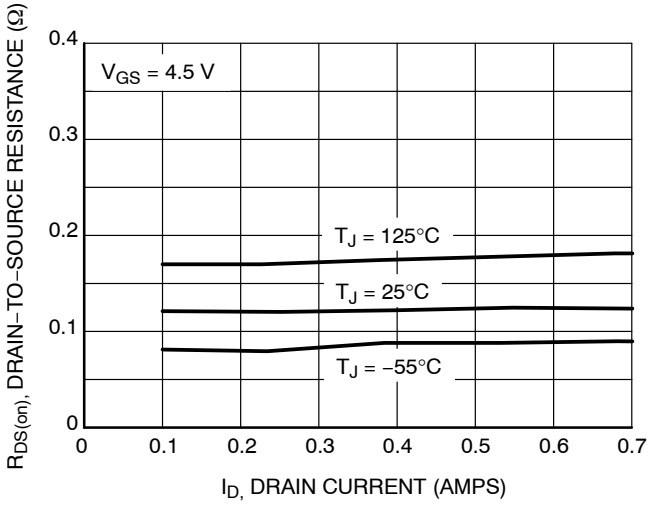


Figure 3. On−Resistance vs. Drain Current and Temperature

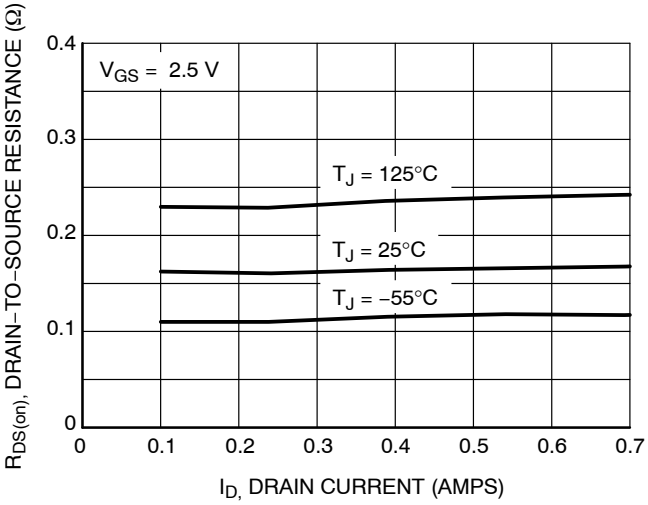


Figure 4. On−Resistance vs. Drain Current and Temperature

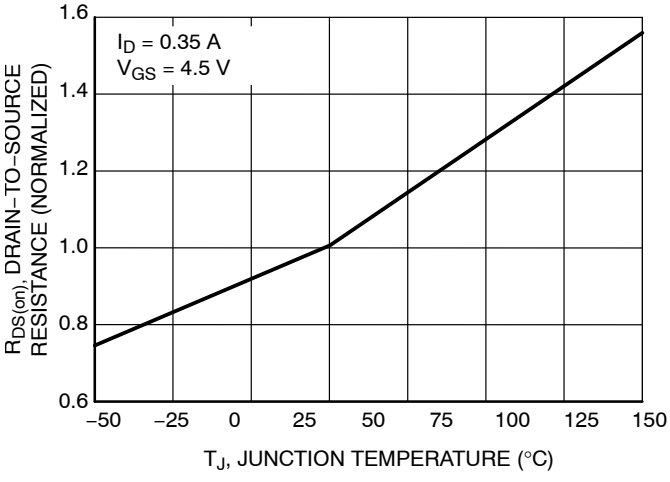


Figure 5. On−Resistance Variation with Temperature

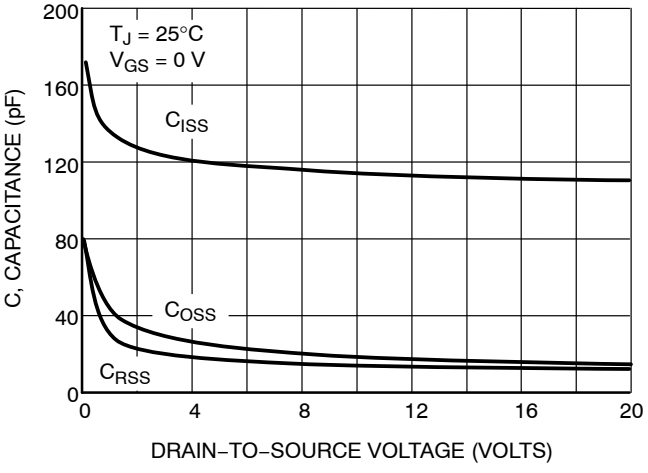


Figure 6. Capacitance Variation

TYPICAL ELECTRICAL CHARACTERISTICS

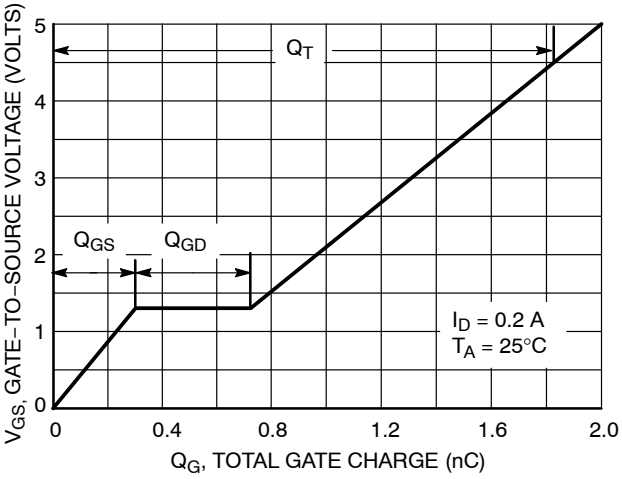


Figure 7. Gate−to−Source Voltage vs. Total Gate Charge

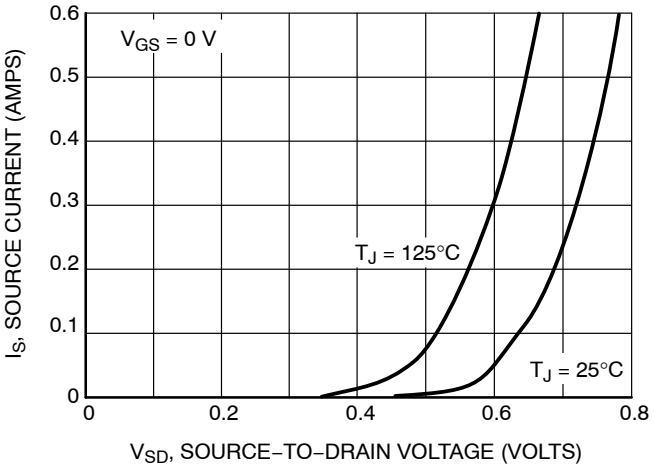


Figure 8. Diode Forward Voltage vs. Current

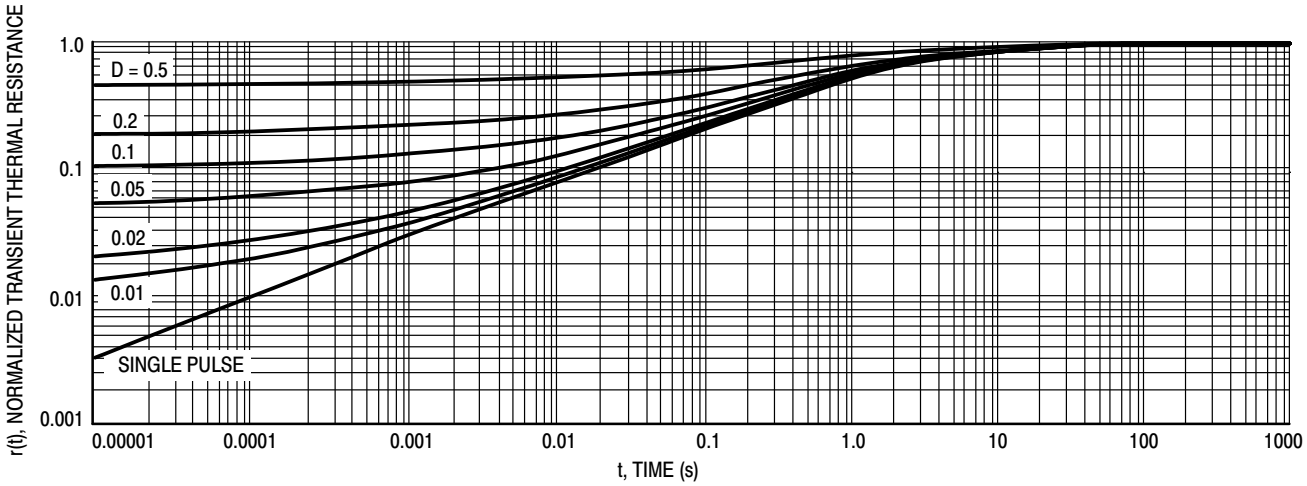


Figure 9. Normalized Thermal Response

ORDERING INFORMATION

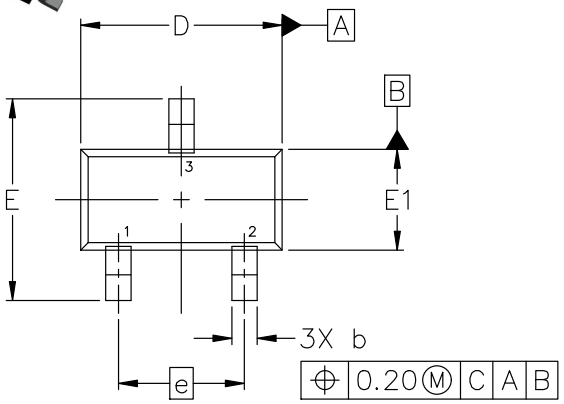
Device	Marking	Package	Shipping†
NTA4153NT1	TR	SC−75 / SOT−416	3000 / Tape & Reel
NTA4153NT1G	TR	SC−75 / SOT−416 (Pb−Free)	3000 / Tape & Reel
NTE4153NT1G	TP	SC−89 (Pb−Free)	3000 / Tape & Reel
NVA4153NT1G	VR	SC−75 / SOT−416 (Pb−Free)	3000 / Tape & Reel
NVE4153NT1G	VP	SC−89 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

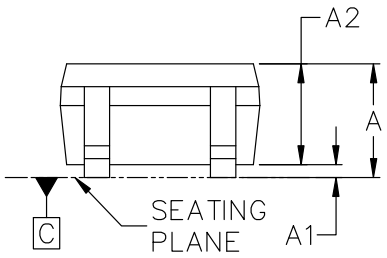
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SC75−3 1.60x0.80x0.80, 1.00P
CASE 463
ISSUE H

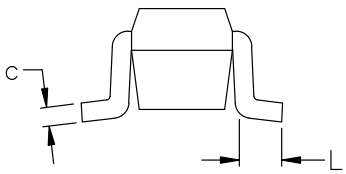
DATE 01 FEB 2024



TOP VIEW



SIDE VIEW



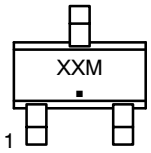
END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.

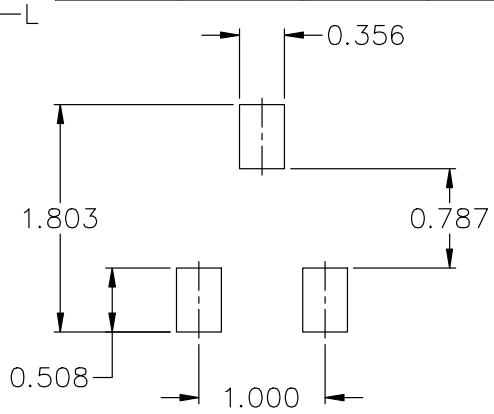
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.80	0.90
A1	0.00	0.05	0.10
A2		0.80 REF.	
b	0.15	0.20	0.30
c	0.10	0.15	0.25
D	1.55	1.60	1.65
E	1.50	1.60	1.70
E1	0.70	0.80	0.90
e		1.00 BSC	
L	0.10	0.15	0.20

GENERIC
MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. GATE
2. SOURCE
3. DRAIN

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DESCRIPTION:	SC75−3 1.60x0.80x0.80, 1.00P	PAGE 1 OF 1

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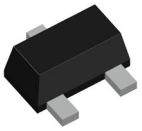
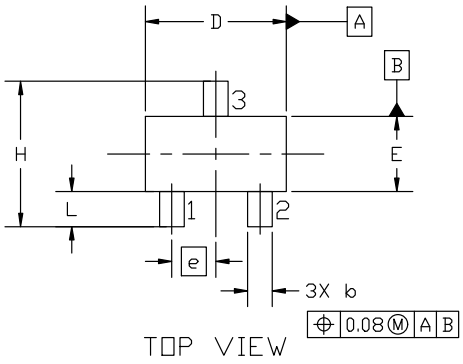
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

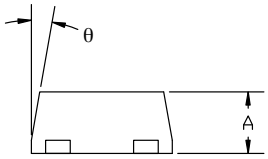


SC−89 3LEAD 1.60x0.85x0.70, 0.50P
CASE 463C
ISSUE D

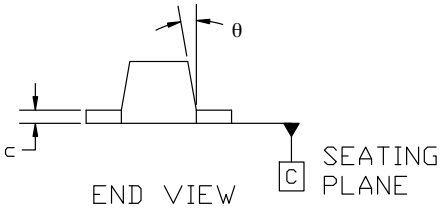
DATE 20 FEB 2024



TOP VIEW



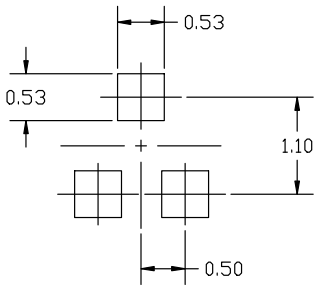
SIDE VIEW



END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.60	0.70	0.80
b	0.23	0.28	0.33
c	0.10	0.15	0.20
D	1.50	1.60	1.70
E	0.75	0.85	0.95
e	0.50 BSC		
H	1.50	1.60	1.70
L	0.30	0.40	0.50
θ	---	---	10°



RECOMMENDED MOUNTING FOOTPRINT

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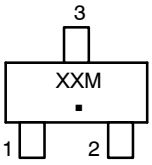
GENERIC MARKING DIAGRAM*



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M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
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3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

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DESCRIPTION:	**SC−89 3LEAD 1.60x0.85x0.70, 0.50P**		**PAGE 1 OF 1**

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- Shortage Management
- Alternative Solution
- Excess Inventory Management