



THE DATASHEET OF LM6172IM



LM6172 Dual High Speed, Low Power, Low Distortion, Voltage Feedback Amplifiers

Check for Samples: [LM6172](#)

FEATURES

- (Typical Unless Otherwise Noted)
- Easy to Use Voltage Feedback Topology
- High Slew Rate 3000V/μs
- Wide Unity-Gain Bandwidth 100MHz
- Low Supply Current 2.3mA/Channel
- High Output Current 50mA/channel
- Specified for ±15V and ±5V Operation

APPLICATIONS

- Scanner I-to-V Converters
- ADSL/HDSL Drivers
- Multimedia Broadcast Systems
- Video Amplifiers
- NTSC, PAL and SECAM Systems
- ADC/DAC Buffers
- Pulse Amplifiers and Peak Detectors

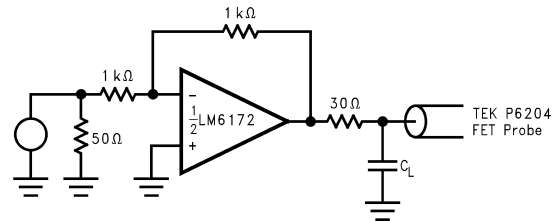
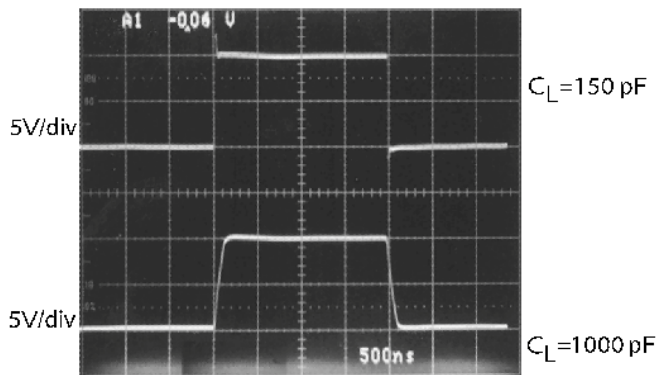
DESCRIPTION

The LM6172 is a dual high speed voltage feedback amplifier. It is unity-gain stable and provides excellent DC and AC performance. With 100MHz unity-gain bandwidth, 3000V/μs slew rate and 50mA of output current per channel, the LM6172 offers high performance in dual amplifiers; yet it only consumes 2.3mA of supply current each channel.

The LM6172 operates on ±15V power supply for systems requiring large voltage swings, such as ADSL, scanners and ultrasound equipment. It is also specified at ±5V power supply for low voltage applications such as portable video systems.

The LM6172 is built with TI's advanced VIP III (Vertically Integrated PNP) complementary bipolar process. See the LM6171 datasheet for a single amplifier with these same features.

LM6172 Driving Capacitive Load



Connection Diagram

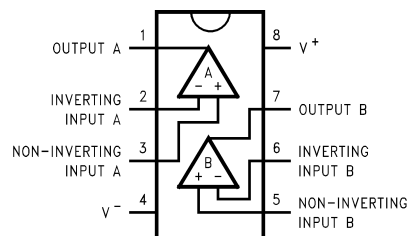


Figure 1. Top View 8-Pin
See Package Numbers P (PDIP) and D (SOIC)



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

ESD Tolerance ⁽³⁾	Human Body Model	3kV
	Machine Model	300V
Supply Voltage ($V^+ - V^-$)		36V
Differential Input Voltage		$\pm 10V$
Common Mode Voltage Range		$V^+ +0.3V$ to $V^- -0.3V$
Input Current		$\pm 10mA$
Output Short Circuit to Ground ⁽⁴⁾		Continuous
Storage Temp. Range		$-65^\circ C$ to $+150^\circ C$
Maximum Junction Temperature ⁽⁵⁾		$150^\circ C$
Soldering Information	Infrared or Convection Reflow (20 sec.)	$235^\circ C$
	Wave Soldering Lead Temp (10 sec.)	$260^\circ C$

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) Human body model, 1.5k Ω in series with 100pF. Machine Model, 200 Ω in series with 100pF.
- (4) Continuous short circuit operation can result in exceeding the maximum allowed junction temperature of $150^\circ C$.
- (5) The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Operating Ratings⁽¹⁾

Supply Voltage		$5.5V \leq V_S \leq 36V$
Operating Temperature Range	LM6172I	$-40^\circ C$ to $+85^\circ C$
Thermal Resistance (θ_{JA})	P Package, 8-Pin PDIP	$95^\circ C/W$
	D Package, 8-Pin SOIC	$160^\circ C/W$

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

$\pm 15V$ DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ C$, $V^+ = +15V$, $V^- = -15V$, $V_{CM} = 0V$, and $R_L = 1k\Omega$. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (1)	LM6172I Limit (2)	Units
V_{OS}	Input Offset Voltage		0.4	3	mV
				4	max
$TC V_{OS}$	Input Offset Voltage Average Drift		6		$\mu V/^\circ C$
I_B	Input Bias Current		1.2	3	μA
				4	max
I_{OS}	Input Offset Current		0.02	2	μA
				3	max
R_{IN}	Input Resistance	Common Mode	40		M Ω
		Differential Mode	4.9		
R_O	Open Loop Output Resistance		14		Ω

- (1) Typical Values represent the most likely parametric normal.
- (2) All limits are guaranteed by testing or statistical analysis.

±15V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = +15\text{V}$, $V^- = -15\text{V}$, $V_{\text{CM}} = 0\text{V}$, and $R_L = 1\text{k}\Omega$. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (1)	LM6172I Limit (2)	Units
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = \pm 10\text{V}$	110	70 65	dB min
PSRR	Power Supply Rejection Ratio	$V_S = \pm 15\text{V}$ to $\pm 5\text{V}$	95	75 70	dB min
V_{CM}	Input Common Mode Voltage Range	CMRR $\geq 60\text{dB}$	± 13.5		V
A_V	Large Signal Voltage Gain ⁽³⁾	$R_L = 1\text{k}\Omega$	86	80 75	dB min
		$R_L = 100\Omega$	78	65 60	dB min
V_O	Output Swing	$R_L = 1\text{k}\Omega$	13.2	12.5 12	V min
			-13.1	-12.5 -12	V max
		$R_L = 100\Omega$	9	6 5	V min
			-8.5	-6 -5	V max
	Continuous Output Current	Sourcing, $R_L = 100\Omega$	90	60 50	mA min
	(Open Loop) ⁽⁴⁾	Sinking, $R_L = 100\Omega$	-85	-60 -50	mA max
I_{SC}	Current Output Short Circuit	Sourcing	107		mA
		Sinking	-105		mA
I_S	Supply Current	Both Amplifiers	4.6	8 9	mA max

(3) Large signal voltage gain is the total output swing divided by the input signal required to produce that swing. For $V_S = \pm 15\text{V}$, $V_{\text{OUT}} = \pm 5\text{V}$. For $V_S = \pm 5\text{V}$, $V_{\text{OUT}} = \pm 1\text{V}$.

(4) The open loop output current is the output swing with the 100Ω load resistor divided by that resistor.

±15V AC Electrical Characteristics

Unless otherwise specified, $T_J = 25^\circ\text{C}$, $V^+ = +15\text{V}$, $V^- = -15\text{V}$, $V_{\text{CM}} = 0\text{V}$, and $R_L = 1\text{k}\Omega$

Symbol	Parameter	Conditions	LM6172I Typ (1)	Units
SR	Slew Rate	$A_V = +2$, $V_{\text{IN}} = 13\text{ V}_{\text{PP}}$	3000	V/ μs
		$A_V = +2$, $V_{\text{IN}} = 10\text{ V}_{\text{PP}}$	2500	V/ μs
	Unity-Gain Bandwidth		100	MHz
	-3 dB Frequency	$A_V = +1$	160	MHz
		$A_V = +2$	62	MHz
	Bandwidth Matching between Channels		2	MHz
Φ_m	Phase Margin		40	Deg
t_s	Settling Time (0.1%)	$A_V = -1$, $V_{\text{OUT}} = \pm 5\text{V}$, $R_L = 500\Omega$	65	ns
A_D	Differential Gain ⁽²⁾		0.28	%
Φ_D	Differential Phase ⁽²⁾		0.6	Deg
e_n	Input-Referred Voltage Noise	$f = 1\text{kHz}$	12	nV/ $\sqrt{\text{Hz}}$
i_n	Input-Referred Current Noise	$f = 1\text{kHz}$	1	pA/ $\sqrt{\text{Hz}}$
	Second Harmonic	$f = 10\text{kHz}$	-110	dB
	Distortion ⁽³⁾	$f = 5\text{MHz}$	-50	dB
	Third Harmonic	$f = 10\text{kHz}$	-105	dB
	Distortion ⁽³⁾	$f = 5\text{MHz}$	-50	dB

(1) Typical Values represent the most likely parametric normal.

(2) Differential gain and phase are measured with $A_V = +2$, $V_{\text{IN}} = 1\text{ V}_{\text{PP}}$ at 3.58MHz and both input and output 75 Ω terminated.

(3) Harmonics are measured with $A_V = +2$, $V_{\text{IN}} = 1\text{ V}_{\text{PP}}$ and $R_L = 100\Omega$.

±5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = +5\text{V}$, $V^- = -5\text{V}$, $V_{\text{CM}} = 0\text{V}$, and $R_L = 1\text{ k}\Omega$. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (1)	LM6172I Limit (2)	Units
V_{OS}	Input Offset Voltage		0.1	3 4	mV max
TC V_{OS}	Input Offset Voltage Average Drift		4		$\mu\text{V}/^\circ\text{C}$
I_{B}	Input Bias Current		1.4	2.5 3.5	μA max
I_{OS}	Input Offset Current		0.02	1.5 2.2	μA max
R_{IN}	Input Resistance	Common Mode	40		M Ω
		Differential Mode	4.9		
R_{O}	Output Resistance		14		Ω
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = \pm 2.5\text{V}$	105	70 65	dB min
PSRR	Power Supply Rejection Ratio	$V_{\text{S}} = \pm 15\text{V}$ to $\pm 5\text{V}$	95	75 70	dB min
V_{CM}	Input Common Mode Voltage Range	CMRR $\geq 60\text{dB}$	± 3.7		V
A_{V}	Large Signal Voltage Gain ⁽³⁾	$R_L = 1\text{ k}\Omega$	82	70 65	dB min
		$R_L = 100\Omega$	78	65 60	dB min
V_{O}	Output Swing	$R_L = 1\text{ k}\Omega$	3.4	3.1 3	V min
			-3.3	-3.1 -3	V max
		$R_L = 100\Omega$	2.9	2.5 2.4	V min
			-2.7	-2.4 -2.3	V max
	Continuous Output Current (Open Loop) ⁽⁴⁾	Sourcing, $R_L = 100\Omega$	29	25 24	mA min
		Sinking, $R_L = 100\Omega$	-27	-24 -23	mA max
I_{SC}	Output Short Circuit Current	Sourcing	93		mA
		Sinking	-72		mA
I_{S}	Supply Current	Both Amplifiers	4.4	6 7	mA max

(1) Typical Values represent the most likely parametric normal.

(2) All limits are guaranteed by testing or statistical analysis.

(3) Large signal voltage gain is the total output swing divided by the input signal required to produce that swing. For $V_{\text{S}} = \pm 15\text{V}$, $V_{\text{OUT}} = \pm 5\text{V}$. For $V_{\text{S}} = \pm 5\text{V}$, $V_{\text{OUT}} = \pm 1\text{V}$.

(4) The open loop output current is the output swing with the 100Ω load resistor divided by that resistor.

±5V AC Electrical Characteristics

Unless otherwise specified, $T_J = 25^\circ\text{C}$, $V^+ = +5\text{V}$, $V^- = -5\text{V}$, $V_{\text{CM}} = 0\text{V}$, and $R_L = 1\text{ k}\Omega$.

Symbol	Parameter	Conditions	LM61722 Typ (1)	Units
SR	Slew Rate	$A_V = +2$, $V_{\text{IN}} = 3.5\text{ V}_{\text{PP}}$	750	V/ μs
	Unity-Gain Bandwidth		70	MHz
	-3 dB Frequency	$A_V = +1$	130	MHz
		$A_V = +2$	45	MHz
ϕ_m	Phase Margin		57	Deg
t_s	Settling Time (0.1%)	$A_V = -1$, $V_{\text{OUT}} = \pm 1\text{V}$, $R_L = 500\Omega$	72	ns
A_D	Differential Gain ⁽²⁾		0.4	%
ϕ_D	Differential Phase ⁽²⁾		0.7	Deg
e_n	Input-Referred Voltage Noise	$f = 1\text{ kHz}$	11	nV/ $\sqrt{\text{Hz}}$
i_n	Input-Referred Current Noise	$f = 1\text{ kHz}$	1	pA/ $\sqrt{\text{Hz}}$
	Second Harmonic Distortion ⁽³⁾	$f = 10\text{ kHz}$	-110	dB
		$f = 5\text{ MHz}$	-48	dB
	Third Harmonic Distortion ⁽³⁾	$f = 10\text{ kHz}$	-105	dB
		$f = 5\text{ MHz}$	-50	dB

(1) Typical Values represent the most likely parametric normal.

(2) Differential gain and phase are measured with $A_V = +2$, $V_{\text{IN}} = 1\text{ V}_{\text{PP}}$ at 3.58MHz and both input and output 75 Ω terminated.

(3) Harmonics are measured with $A_V = +2$, $V_{\text{IN}} = 1\text{ V}_{\text{PP}}$ and $R_L = 100\Omega$.

Typical Performance Characteristics

unless otherwise noted, $T_A = 25^\circ\text{C}$

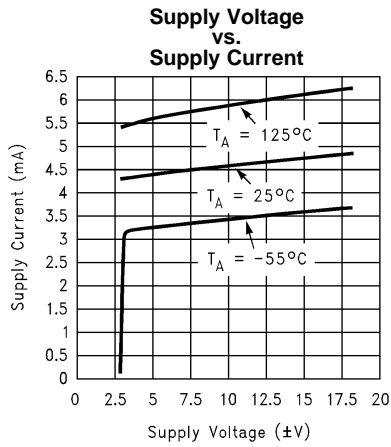


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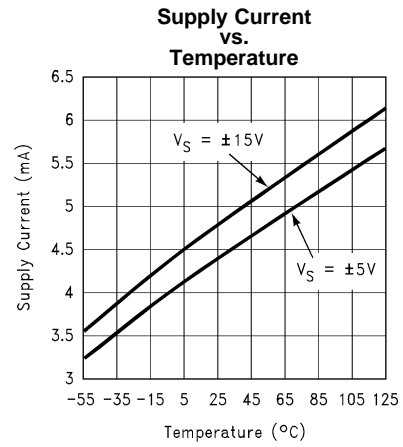


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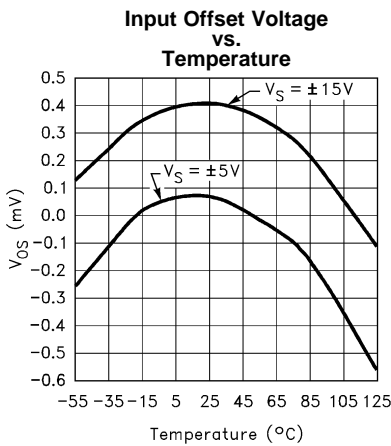


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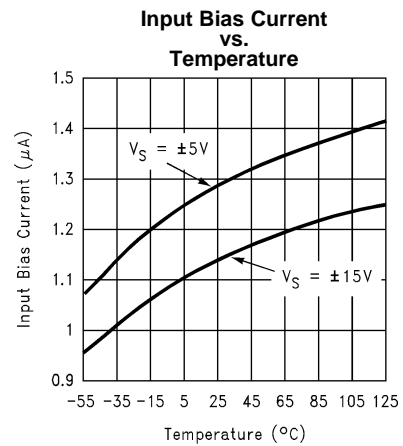


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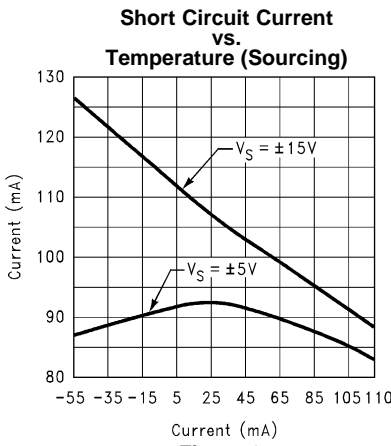


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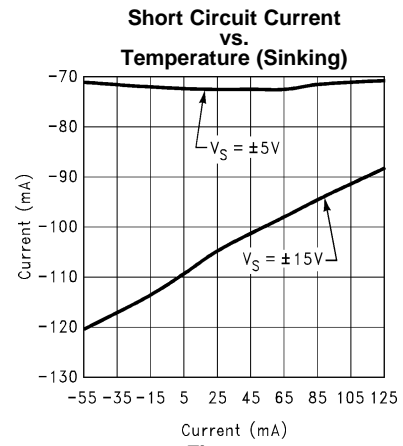


Figure 7.

Typical Performance Characteristics (continued)

unless otherwise noted, $T_A = 25^\circ\text{C}$

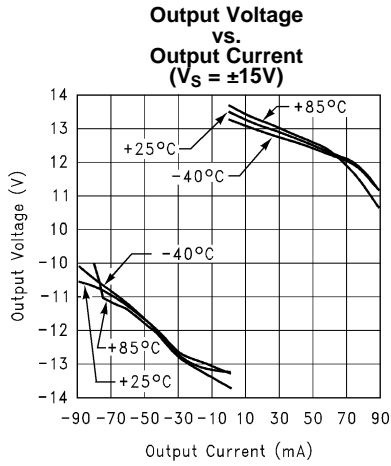


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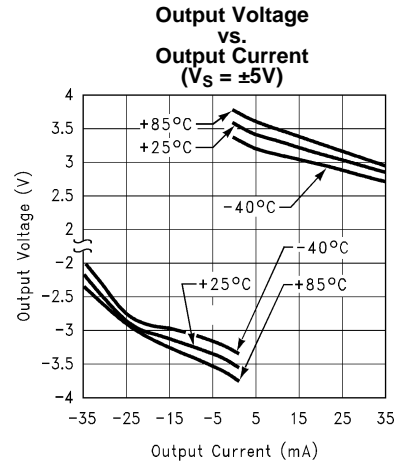


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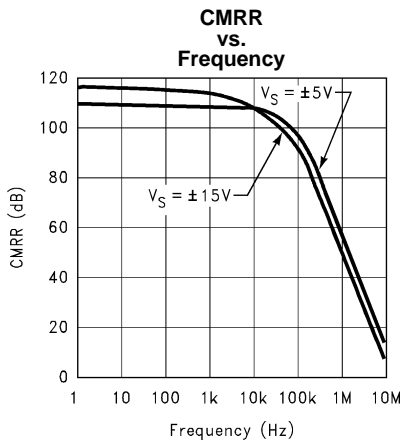


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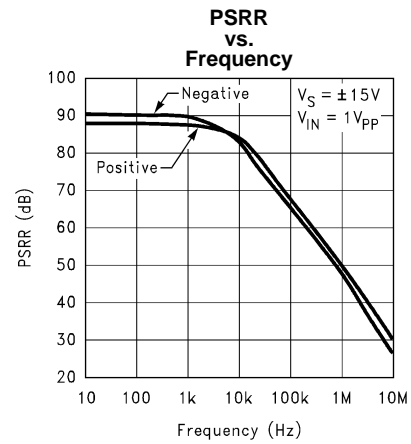


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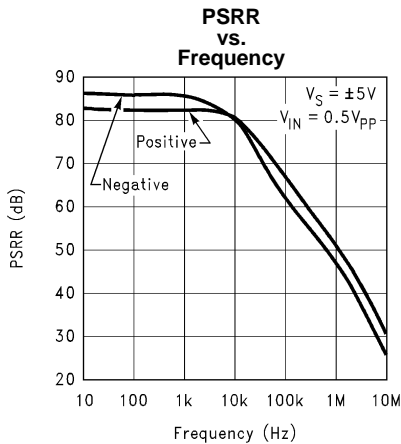


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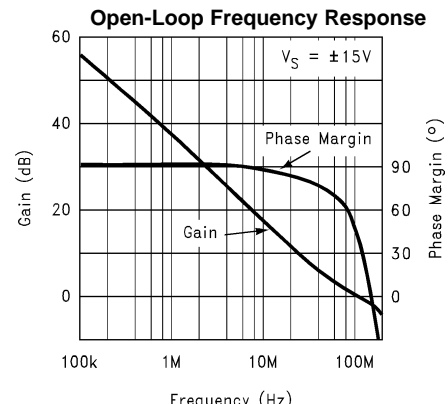


Figure 13.

Typical Performance Characteristics (continued)

unless otherwise noted, $T_A = 25^\circ\text{C}$

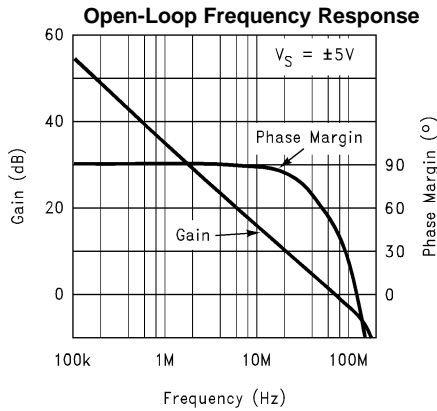


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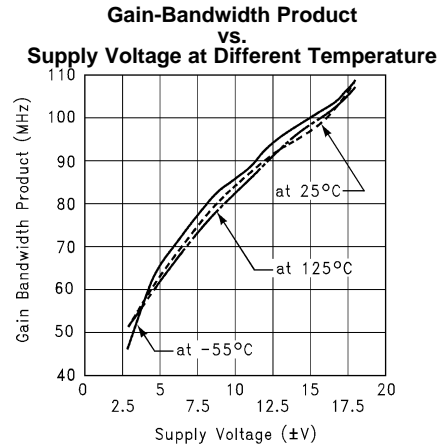


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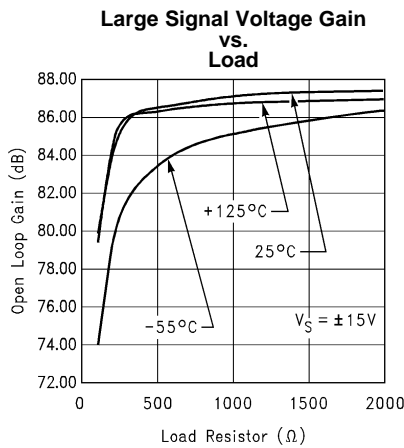


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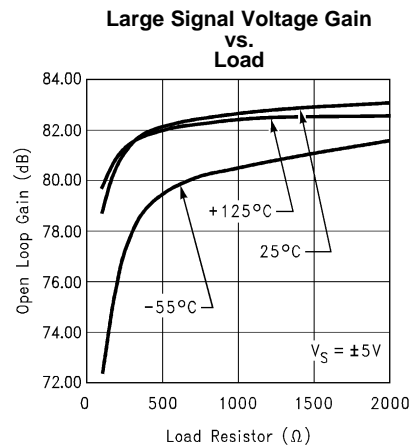


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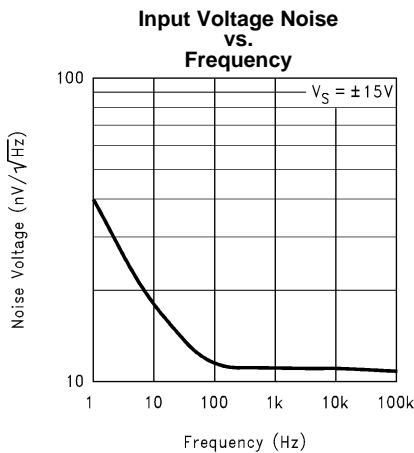


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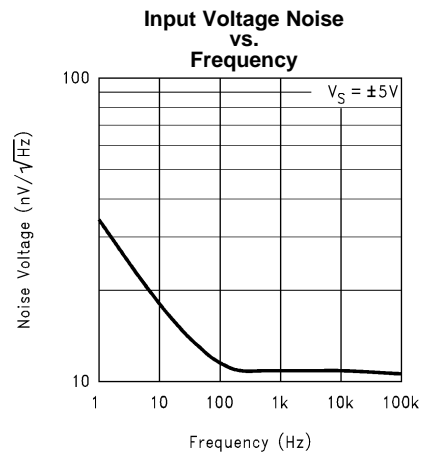


Figure 19.

Typical Performance Characteristics (continued)

unless otherwise noted, $T_A = 25^\circ\text{C}$

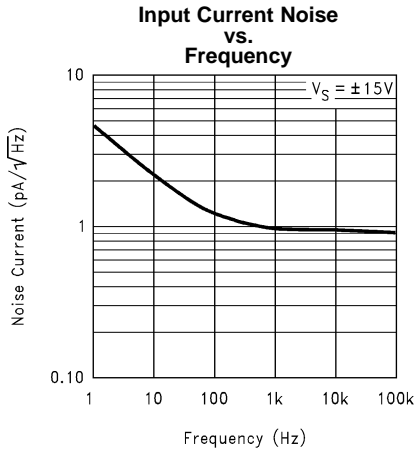


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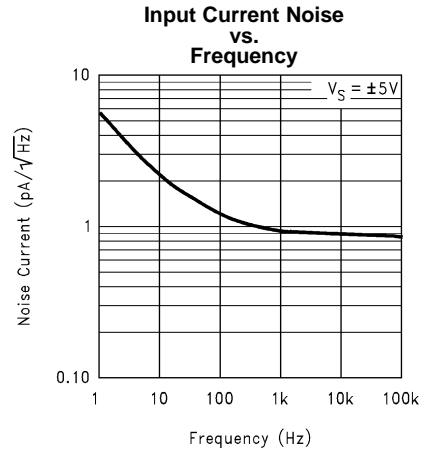


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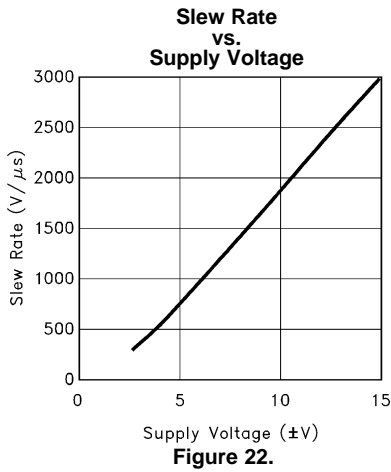


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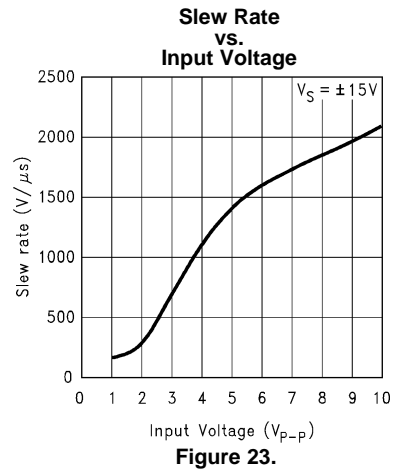


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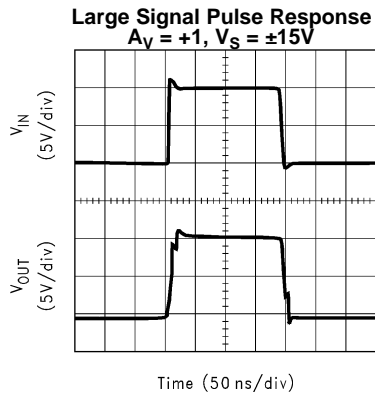


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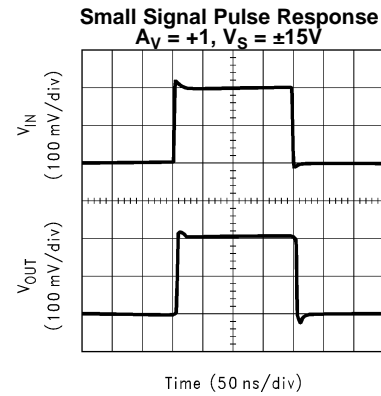
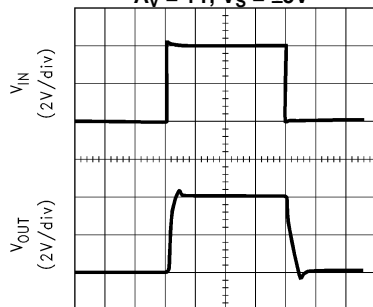


Figure 25.

Typical Performance Characteristics (continued)

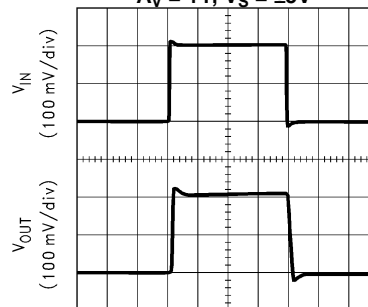
unless otherwise noted, $T_A = 25^\circ\text{C}$

Large Signal Pulse Response
 $A_V = +1, V_S = \pm 5\text{V}$



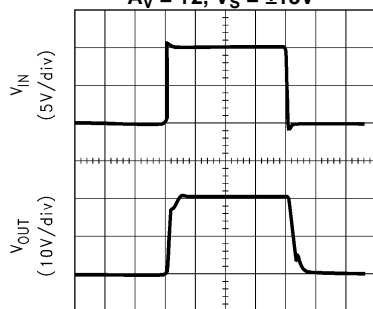
Time (50 ns/div)
Figure 26.

Small Signal Pulse Response
 $A_V = +1, V_S = \pm 5\text{V}$



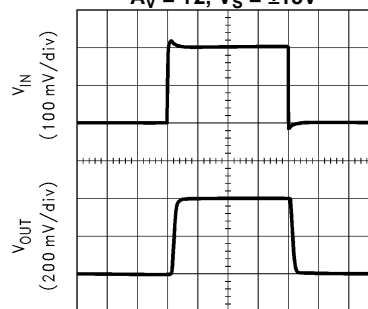
Time (50 ns/div)
Figure 27.

Large Signal Pulse Response
 $A_V = +2, V_S = \pm 15\text{V}$



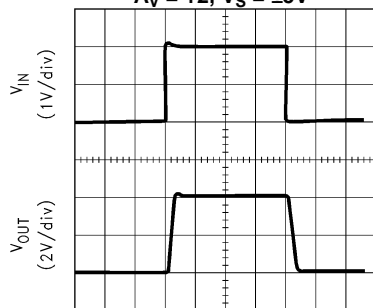
Time (50 ns/div)
Figure 28.

Small Signal Pulse Response
 $A_V = +2, V_S = \pm 15\text{V}$



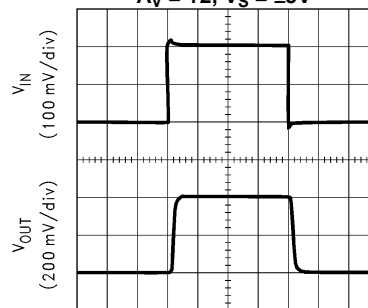
Time (50 ns/div)
Figure 29.

Large Signal Pulse Response
 $A_V = +2, V_S = \pm 5\text{V}$



Time (50 ns/div)
Figure 30.

Small Signal Pulse Response
 $A_V = +2, V_S = \pm 5\text{V}$

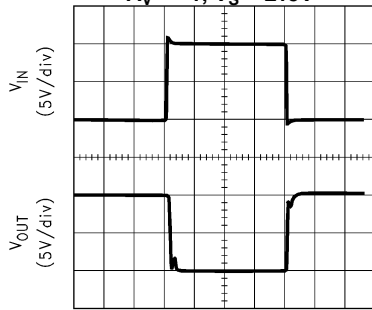


Time (50 ns/div)
Figure 31.

Typical Performance Characteristics (continued)

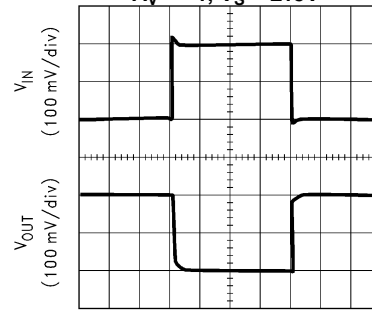
unless otherwise noted, $T_A = 25^\circ\text{C}$

Large Signal Pulse Response
 $A_V = -1, V_S = \pm 15\text{V}$



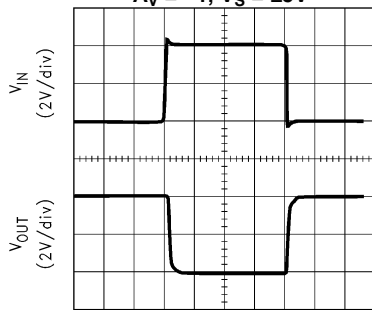
Time (50 ns/div)
Figure 32.

Small Signal Pulse Response
 $A_V = -1, V_S = \pm 15\text{V}$



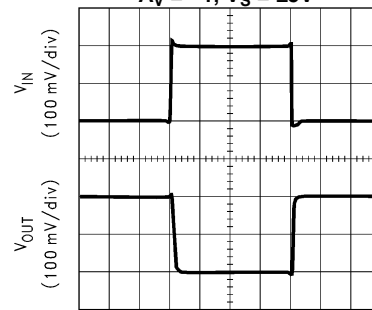
Time (50 ns/div)
Figure 33.

Large Signal Pulse Response
 $A_V = -1, V_S = \pm 5\text{V}$



Time (50 ns/div)
Figure 34.

Small Signal Pulse Response
 $A_V = -1, V_S = \pm 5\text{V}$



Time (50 ns/div)
Figure 35.

Closed Loop Frequency Response vs. Supply Voltage
 $(A_V = +1)$

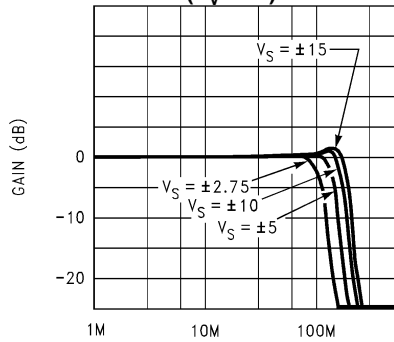


Figure 36.

Closed Loop Frequency Response vs. Supply Voltage
 $(A_V = +2)$

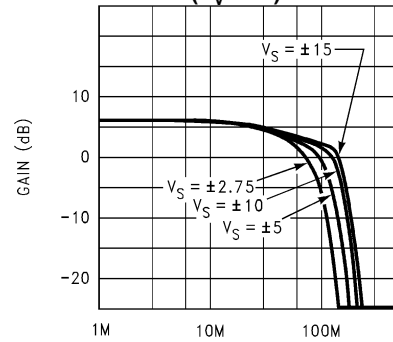


Figure 37.

Typical Performance Characteristics (continued)

unless otherwise noted, $T_A = 25^\circ\text{C}$

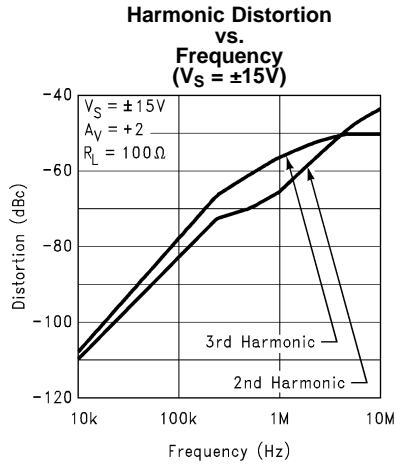


Figure 38.

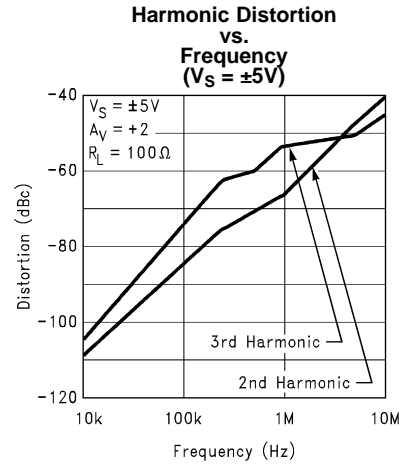


Figure 39.

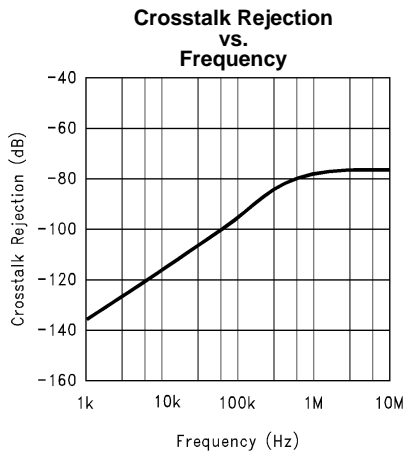


Figure 40.

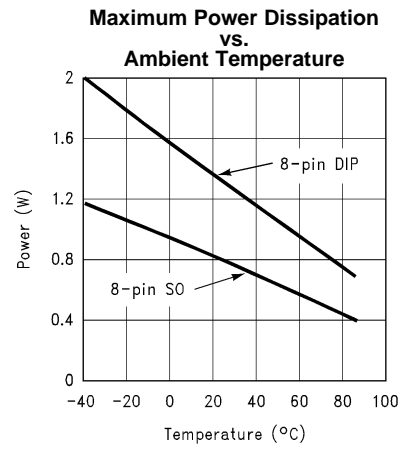


Figure 41.

LM6172 Simplified Schematic (Each Amplifier)

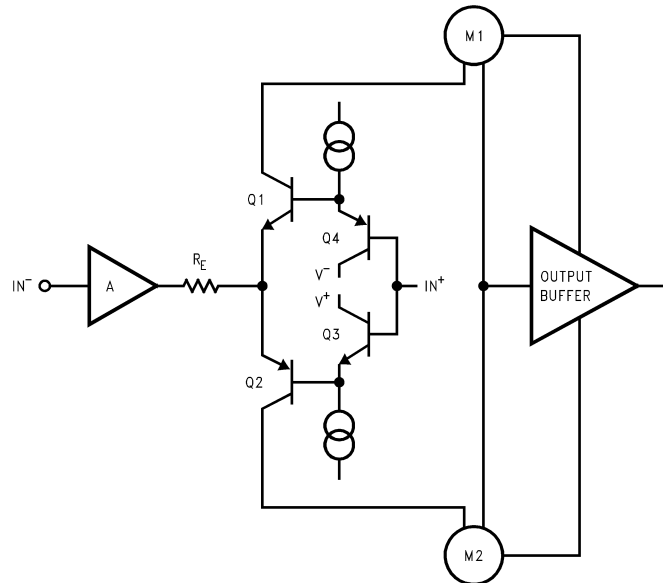


Figure 42.

APPLICATION NOTES

LM6172 PERFORMANCE DISCUSSION

The LM6172 is a dual high-speed, low power, voltage feedback amplifier. It is unity-gain stable and offers outstanding performance with only 2.3mA of supply current per channel. The combination of 100MHz unity-gain bandwidth, 3000V/ μ s slew rate, 50mA per channel output current and other attractive features makes it easy to implement the LM6172 in various applications. Quiescent power of the LM6172 is 138mW operating at \pm 15V supply and 46mW at \pm 5V supply.

LM6172 CIRCUIT OPERATION

The class AB input stage in LM6172 is fully symmetrical and has a similar slewing characteristic to the current feedback amplifiers. In Figure 42, Q1 through Q4 form the equivalent of the current feedback input buffer, R_E the equivalent of the feedback resistor, and stage A buffers the inverting input. The triple-buffered output stage isolates the gain stage from the load to provide low output impedance.

LM6172 SLEW RATE CHARACTERISTIC

The slew rate of LM6172 is determined by the current available to charge and discharge an internal high impedance node capacitor. This current is the differential input voltage divided by the total degeneration resistor R_E . Therefore, the slew rate is proportional to the input voltage level, and the higher slew rates are achievable in the lower gain configurations.

When a very fast large signal pulse is applied to the input of an amplifier, some overshoot or undershoot occurs. By placing an external series resistor such as 1k Ω to the input of LM6172, the slew rate is reduced to help lower the overshoot, which reduces settling time.

REDUCING SETTling TIME

The LM6172 has a very fast slew rate that causes overshoot and undershoot. To reduce settling time on LM6172, a 1k Ω resistor can be placed in series with the input signal to decrease slew rate. A feedback capacitor can also be used to reduce overshoot and undershoot. This feedback capacitor serves as a zero to increase the stability of the amplifier circuit. A 2pF feedback capacitor is recommended for initial evaluation. When the LM6172 is configured as a buffer, a feedback resistor of 1k Ω must be added in parallel to the feedback capacitor.

Another possible source of overshoot and undershoot comes from capacitive load at the output. Please see [DRIVING CAPACITIVE LOADS](#) for more detail.

DRIVING CAPACITIVE LOADS

Amplifiers driving capacitive loads can oscillate or have ringing at the output. To eliminate oscillation or reduce ringing, an isolation resistor can be placed as shown in [Figure 43](#). The combination of the isolation resistor and the load capacitor forms a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of the isolation resistor; the bigger the isolation resistor, the more damped (slow) the pulse response becomes. For LM6172, a 50Ω isolation resistor is recommended for initial evaluation.

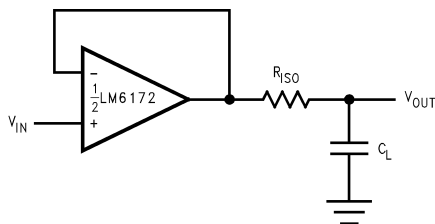


Figure 43. Isolation Resistor Used to Drive Capacitive Load

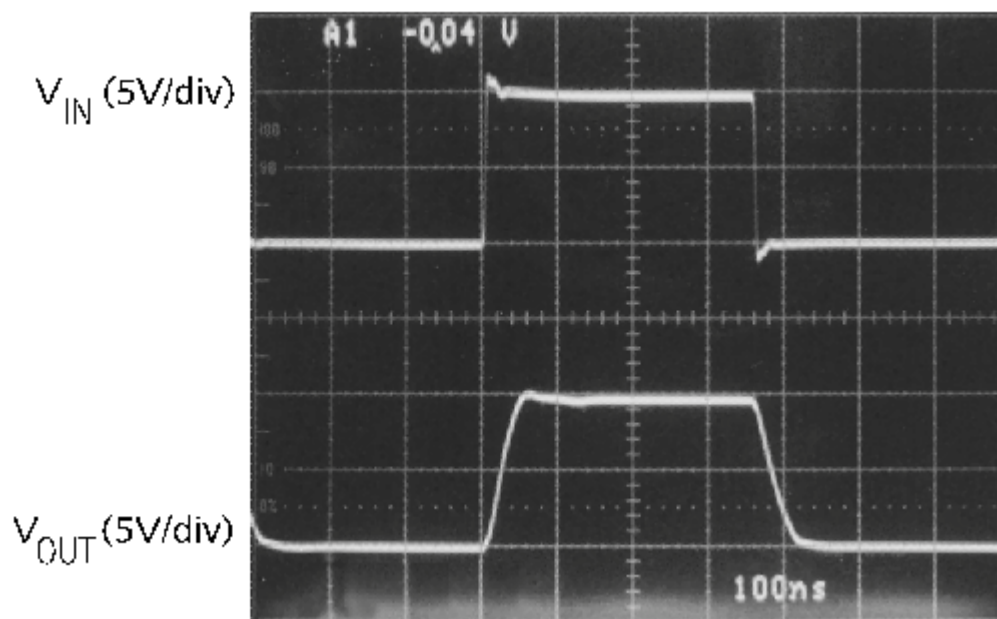


Figure 44. The LM6172 Driving a 510pF Load with a 30Ω Isolation Resistor

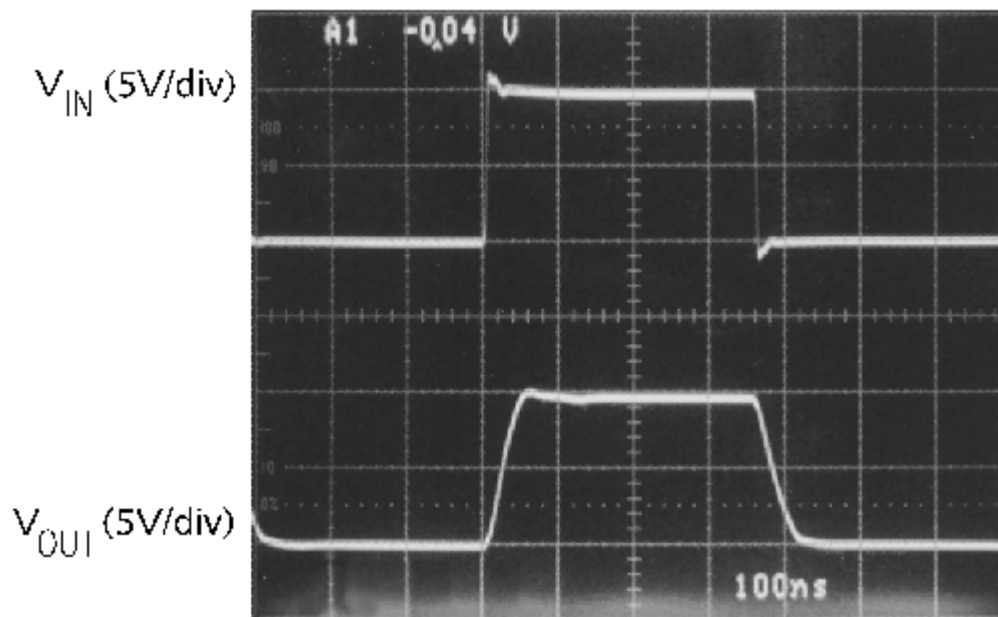


Figure 45. The LM6172 Driving a 220 pF Load with a 50Ω Isolation Resistor

LAYOUT CONSIDERATION

PRINTED CIRCUIT BOARDS AND HIGH SPEED OP AMPS

There are many things to consider when designing PC boards for high speed op amps. Without proper caution, it is very easy to have excessive ringing, oscillation and other degraded AC performance in high speed circuits. As a rule, the signal traces should be short and wide to provide low inductance and low impedance paths. Any unused board space needs to be grounded to reduce stray signal pickup. Critical components should also be grounded at a common point to eliminate voltage drop. Sockets add capacitance to the board and can affect frequency performance. It is better to solder the amplifier directly into the PC board without using any socket.

USING PROBES

Active (FET) probes are ideal for taking high frequency measurements because they have wide bandwidth, high input impedance and low input capacitance. However, the probe ground leads provide a long ground loop that will produce errors in measurement. Instead, the probes can be grounded directly by removing the ground leads and probe jackets and using scope probe jacks.

COMPONENTS SELECTION AND FEEDBACK RESISTOR

It is important in high speed applications to keep all component leads short because wires are inductive at high frequency. For discrete components, choose carbon composition-type resistors and mica-type capacitors. Surface mount components are preferred over discrete components for minimum inductive effect.

Large values of feedback resistors can couple with parasitic capacitance and cause undesirable effects such as ringing or oscillation in high speed amplifiers. For LM6172, a feedback resistor less than 1kΩ gives optimal performance.

COMPENSATION FOR INPUT CAPACITANCE

The combination of an amplifier's input capacitance with the gain setting resistors adds a pole that can cause peaking or oscillation. To solve this problem, a feedback capacitor with a value

$$C_F > (R_G \times C_{IN})/R_F \quad (1)$$

can be used to cancel that pole. For LM6172, a feedback capacitor of 2pF is recommended. [Figure 46](#) illustrates the compensation circuit.

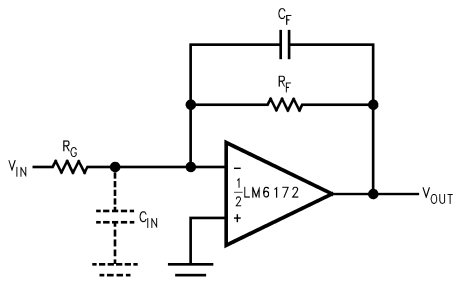


Figure 46. Compensating for Input Capacitance

POWER SUPPLY BYPASSING

Bypassing the power supply is necessary to maintain low power supply impedance across frequency. Both positive and negative power supplies should be bypassed individually by placing 0.01 μ F ceramic capacitors directly to power supply pins and 2.2 μ F tantalum capacitors close to the power supply pins.

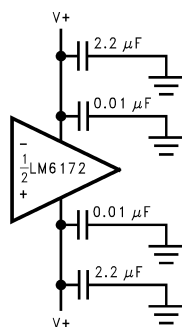


Figure 47. Power Supply Bypassing

TERMINATION

In high frequency applications, reflections occur if signals are not properly terminated. [Figure 48](#) shows a properly terminated signal while [Figure 49](#) shows an improperly terminated signal.

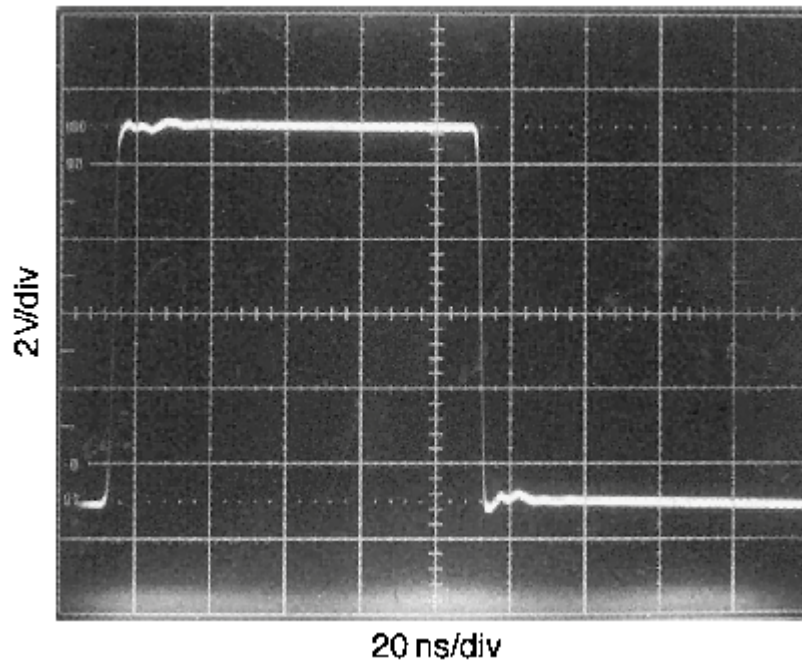


Figure 48. Properly Terminated Signal

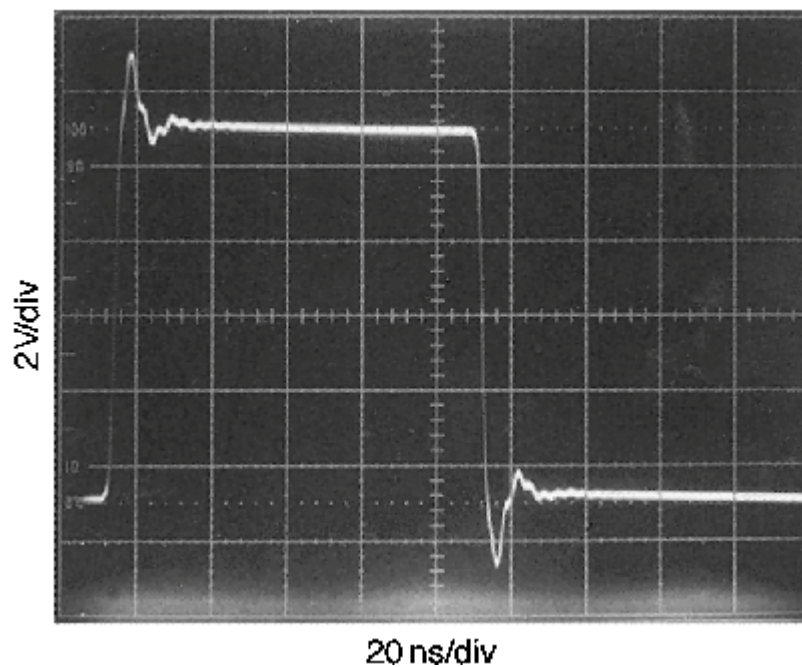


Figure 49. Improperly Terminated Signal

To minimize reflection, coaxial cable with matching characteristic impedance to the signal source should be used. The other end of the cable should be terminated with the same value terminator or resistor. For the commonly used cables, RG59 has 75Ω characteristic impedance, and RG58 has 50Ω characteristic impedance.

POWER DISSIPATION

The maximum power allowed to dissipate in a device is defined as:

$$P_D = (T_{J(max)} - T_A) / \theta_{JA}$$

Where

- P_D is the power dissipation in a device
- $T_{J(max)}$ is the maximum junction temperature
- T_A is the ambient temperature
- θ_{JA} is the thermal resistance of a particular package

For example, for the LM6172 in a SOIC-8 package, the maximum power dissipation at 25°C ambient temperature is 780mW.

Thermal resistance, θ_{JA} , depends on parameters such as die size, package size and package material. The smaller the die size and package, the higher θ_{JA} becomes. The 8-pin DIP package has a lower thermal resistance (95°C/W) than that of 8-pin SO (160°C/W). Therefore, for higher dissipation capability, use an 8-pin DIP package.

The total power dissipated in a device can be calculated as: $P_D = P_Q + P_L$ (2)

P_Q is the quiescent power dissipated in a device with no load connected at the output. P_L is the power dissipated in the device with a load connected at the output; it is not the power dissipated by the load.

Furthermore,

$P_Q =$ supply current x total supply voltage with no load

$P_L =$ output current x (voltage difference between supply voltage and output voltage of the same supply)

For example, the total power dissipated by the LM6172 with $V_S = \pm 15V$ and both channels swinging output voltage of 10V into 1kΩ is

$$\begin{aligned}
 P_D &= P_Q + P_L \\
 &= 2[(2.3mA)(30V)] + 2[(10mA)(15V - 10V)] \\
 &= 138mW + 100mW \\
 &= 238mW
 \end{aligned}$$

Application Circuits

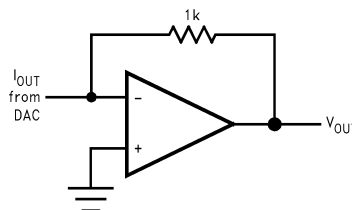


Figure 50. I-to-V Converters

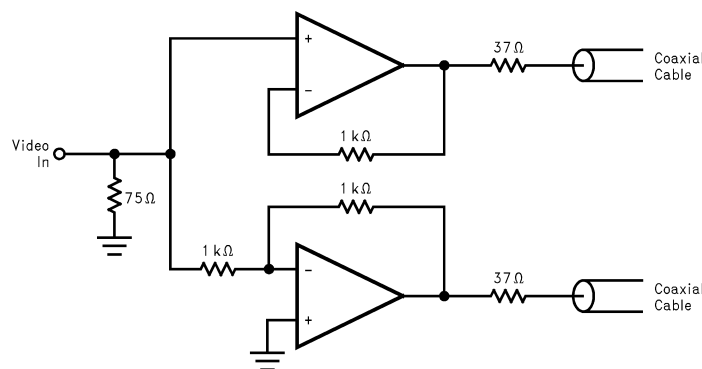


Figure 51. Differential Line Driver

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	19

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM6172IM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LM61 72IM	
LM6172IM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM61 72IM	Samples
LM6172IMX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LM61 72IM	
LM6172IMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM61 72IM	Samples
LM6172IN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN Call TI	Level-1-NA-UNLIM	-40 to 85	LM6172IN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM6172IMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6172IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM6172IMX	SOIC	D	8	2500	367.0	367.0	35.0
LM6172IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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